IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant | : Hisashi Ohtani et al. | Art Unit | : 2815 |
| Serial No. | : 09/379,702 | Examiner | : Eugene Lee |
| Filed | : August 24, 1999 | Conf. No. | : 1613 |
| Title | : METHOD OF FABRICATING SEMICONDUCTOR DEVICES | | |

**MAIL STOP RCE**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Supplemental to the Information Disclosure Statements filed on August 24, 1999 and September 27, 1999, applicants submit the attached corrected Forms PTO-1449. All of the documents (Desig. ID. "A"-"H" and "M"-"S") listed on the Corrected Form PTO-1449 were originally cited in the parent application and attached to the divisional application transmittal on August 24, 1999. This Corrected Form PTO-1449 is being submitted to correct the format of the submission of documents previously cited in a parent application. The second corrected Form PTO-1449 is being submitted to correct a typographical error in the description of the reference identified as Desig. ID "AL" and was submitted with the Information Disclosure Statement filed on September 27, 1999. Please note that, for this reference, the translation has been included as "ABS" to indicate that an abstract was included with the foreign language reference.

No fees are believed due. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/23/09

John F. Hayden
Reg. No. 37640

Customer No. 26171
Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (877) 769-7945